

REMARKS

Claims 1-10 and 12-18 are all the claims pending in the application.

I. Claim Rejections under 35 U.S.C. § 102

A. The Examiner has rejected claims 1-3 and 10-13 under 35 U.S.C. § 102(b) as being anticipated by Fujinami et al. (U.S. 5,568,274).

Claim 1 recites the features of a matching status information outputter operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of a packet start code; a formatter operable to output predetermined data in accordance with matching status information, wherein, when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code. Applicants submit that Fujinami fails to disclose or suggest such a combination of features.

Initially, with respect to the rejection of claim 1, Applicants note that the main difference between the present Office Action and the Office Action dated August 25, 2005 pertains to the above-noted feature drawn to a matching status information outputter that is operable to “output matching status information at a head part of a packet start code.”

In particular, in the present Office Action, the Examiner has taken the position that Fujinami discloses such a feature at col. 10, lines 51-56 and in Fig. 26 (see Office Action at page 4). Applicants note, however, that col. 10, lines 51-56 of Fujinami is in the Brief Description of the Drawings section of the reference and merely provides a general description of Figs. 2-4, and

in no way whatsoever relates to a CIP header as discussed in the Office Action. Further, Applicants note that Fujinami does not include a Fig. 26. Rather, Fujinami only includes Figs. 1-19.

In view of the foregoing, Applicants respectfully submit that the Examiner's rejection of claim 1 is clearly improper because the portion of Fujinami which was relied on in the Office Action does not disclose anything related to a CIP header, as was indicated in the Office Action, and because Fujinami does not include a Fig. 26, as was also indicated in the Office Action.

Accordingly, as Fujinami does not disclose at least the feature of a matching status information outputter that is operable to "output matching status information at a head part of a packet start code", Applicants respectfully submit that claim 1 is patentable over Fujinami, an indication of which is kindly requested.

Further, with respect to claim 1, Applicants note that the Examiner has not responded to the arguments that were presented in the Appeal Brief dated May 25, 2006. Accordingly, the relevant arguments are presented again below for the Examiner's reference, and the Examiner is kindly requested to consider and address each of these arguments.

Regarding the Fujinami reference, Applicants note that this reference discloses an apparatus for recording multiplexed audio and video signals, wherein the apparatus includes a header separation circuit 22, a switching circuit 23, and a control circuit 24 (see Figs. 2 and 12). The header separation circuit 22 separates pack headers and packet headers from a multiplexed signal, supplies the separated headers to the control circuit 24, and supplies the multiplexed signal to an input terminal G of the switching circuit 23 (see col. 3, lines 9-15).

In Fujinami, the control circuit 24 causes the switching circuit 23 to connect the input terminal G successively to the output terminals H1 and H2 in accordance with a stream ID of the packet header received from the header separation circuit 22 (see col. 3, lines 17-22 and col. 15, lines 29-33). By operating the switching circuit 23 of Fujinami in this manner, the video data and the audio data can be separated from one another, wherein the video data is supplied to the video decoder 25 and the audio data is supplied to the audio decoder 26 (see Figs. 2 and 12; and col. 3, lines 22-25).

In the final Office Action, the Examiner has taken the position that the feature recited in claim 1 of a matching status information outputter that is operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code is disclosed in Fujinami at col. 3, lines 17-22 (see final Office Action at page 4).

In this regard, as noted by the Examiner in the Office Action, col. 3, lines 17-22 of Fujinami recites the following:

The control circuit 24 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output terminals H1 and H2 in accordance with the stream ID of the packet header received from the header separation circuit 22.

Thus, the Examiner has taken the position in the Office Action that the control circuit 24 of Fujinami corresponds to the "matching status information outputter" as recited in claim 1.

Applicants note, however, that with respect to the feature recited in claim 1 of a formatter operable to output predetermined data in accordance with matching status information, the Examiner has taken the position that this feature is also disclosed by Fujinami at col. 3, lines 17-22 (see final Office Action at page 4).

Thus, the Examiner is apparently taking the position that the control circuit 24 of Fujinami corresponds to the "data formatter" of claim 1, and that the control signal which is output from the control circuit 24 corresponds to the "predetermined data" of claim 1. As noted above, however, the Examiner has also taken the position that the control circuit 24 of Fujinami corresponds to the "matching status information outputter" of claim 1.

Applicants submit that such a position is clearly improper. For example, as claim 1 indicates that the data formatter outputs predetermined data in accordance with the matching status information, it is clear that the Examiner's reliance on the control circuit 24 of Fujinami as corresponding to both of the "matching status information outputter" and the "data formatter" of claim 1 is incorrect.

In other words, as the control circuit 24 of Fujinami is merely responsible for outputting a signal which controls the switching circuit 23, Applicants submit that the control circuit 24 cannot correspond to both of a matching status information outputter that outputs matching status information and a data formatter that outputs predetermined data in accordance with matching status information.

Moreover, as noted above, claim 1 recites that when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code. Thus, as is clearly evident from claim 1, this predetermined data is the predetermined data that is output from the "data formatter" of claim 1.

As noted above, the Examiner has taken the position that the output of the control circuit 24 of Fujinami corresponds to the "predetermined data" in claim 1. However, in the final Office Action, it is noted that the Examiner has taken an inconsistent position by indicating that "the predetermined data" that is output so as to be positioned at a head part of the data other than a header which follows the next packet start code corresponds to a "signal-type marker" disclosed by Fujinami at col. 8, lines 64-67 (see final Office Action at page 5).

Applicants note that the signal-type marker of Fujinami is a marker that is located adjacent to a signal portion of a predetermined type so as to identify the signal portion of the predetermined type in a multiplexed signal (see col. 8, lines 29-32 and 64-67). Thus, it is clear that the signal-type marker of Fujinami is not a signal that is output by the control circuit 24 of Fujinami to control the switching circuit 23.

Therefore, as the Examiner has taken the position that "the predetermined data" of claim 1 corresponds to two completely different pieces of data in Fujinami, it is clear that the Examiner has taken an inconsistent position in formulating the rejection of claim 1.

In view of the foregoing, Applicants submit that Fujinami does not disclose, suggest or otherwise render obvious the combination of a matching status information outputter operable to detect a matching status of a code which is input for every predetermined bit with a prefix code of a packet start code, and to output matching status information at a head part of a packet start code; a formatter operable to output predetermined data in accordance with matching status information, wherein, when a next packet start code is recognized, the predetermined data is

output so as to be positioned at a head part of the data other than a header which follows the next packet start code, as recited in claim 1.

Claims 2, 3 and 10-13 depend from claim 1 and are therefore considered patentable at least by virtue of their dependency.

B. The Examiner has rejected claims 8, 9 and 18 under 35 U.S.C. § 102(b) as being anticipated by Yanagihara et al. (U.S. 6,172,989).

Independent claim 8 recites the feature of a formatter operable to add a predetermined number of pseudo data to the rear of a code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data. Applicants submit that the Yanagihara fails to disclose or suggest at least this feature of claim 8.

As explained in Yanagihara, communication of MPEG-PS data is not normally performed by using a digital interface in accordance with IEEE 1394 (see col. 1 lines 17-19 and col. 2, lines 51-55). In order to transmit such data in accordance with IEEE 1394, Yanagihara discloses that a pack forming a unit of MPEG-PS data (which has a length of 2,048 bytes) can be converted into packets that are transmitted in accordance with IEEE 1394 (see col. 3, lines 5-12).

In order to convert the MPEG-PS data into a packet that is transmitted in accordance with the IEEE 1394 standard, padding data is added. For example, in the Abstract of Yanagihara and in col. 7, lines 1-7, it is disclosed that Yanagihara is able to add padding data to a 2,048 byte pack of MPEG-PS data so that the overall byte length of data is a multiple of 16. Thus, in Yanagihara

the padding data is added so that data packets can be divided into data blocks having a size (e.g., 36 byte data blocks as shown in Fig. 16(E)) that is necessary to convert the MPEG-PS data pack into packets that conform with IEEE 1394.

In the Office Action, the Examiner asserts that the above-noted disclosure in Yanagihara related to the adding of padding data is performed for “identical purposes” as Applicants’ invention. Applicants respectfully disagree.

In particular, as explained above, the padding data in Yangihara is added so that data packets can be divided into data blocks having a size that is necessary to convert the MPEG-PS data pack into packets that conform with IEEE 1394. In contrast, according to the present invention, pseudo data is added to the rear of a code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data.

For example, as explained in an illustrative embodiment of the present invention, if the width of a data bus for pipeline transfer is n bytes, when video data of an end part of coded data is positioned at the m -th byte from the bus width boundary, $n-m$ or more pieces of padding data will be added such that the video data of the end part of the coded data can be read by pipeline processing (see the specification at page 36, lines 6-15 and Figs. 6(a), 6(b)).

As discussed above, in Yanagihara, the padding data is merely added so that data packets can be divided into data blocks having a size (e.g., 36 byte data blocks as shown in Fig. 16(E)) that is necessary to convert the MPEG-PS data pack into packets that conform with IEEE 1394. Thus, while the addition of the padding data in Yanagihara is necessary for the above-noted

conversion, the addition of the padding data in Yanagihara is not performed so as to equalize the bus width of a pipeline transfer.

In view of the foregoing, Applicants submit that Yanagihara does not disclose, suggest or otherwise render obvious the feature of a formatter that is operable to add a predetermined number of pseudo data to the rear of a code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data, as recited in claim 8.

Claims 9 and 18 depend from claim 8 are therefore considered patentable at least by virtue of their dependency.

II. Claim Rejections under 35 U.S.C. § 103(a)

A. The Examiner has rejected claims 4, 6, 7, 14, 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Fujinami et al. in view of Boden (U.S. 5,633,686).

Claims 4, 6, 7, 14, 16 and 17 depend from claim 1. Applicants respectfully submit that Boden fails to cure the deficiencies of Fujinami, as discussed above, with respect to claim 1. Accordingly, Applicants submit that claims 4, 6, 7, 14, 16 and 17 are patentable at least by virtue of their dependency.

B. The Examiner has rejected claims 5 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Fujinami et al. in view of Toyohara (U.S. 5,768,265).

Claims 5 and 15 depend from claim 1. Applicants respectfully submit that Toyohara fails to cure the deficiencies of Fujinami, as discussed above, with respect to claim 1. Accordingly, Applicants submit that claims 5 and 15 are patentable at least by virtue of their dependency.

III. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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